Worldwide Technologies and the ITRS in the Current Economic Climate

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Introduction

Development of the key technological elements of the silicon-gate process, that represents the backbone of the semiconductor industry, was completed in the late 60's. By the first half of the 70's the fundamental laws of device scaling were well known. Device scaling is at the foundation of the Semiconductor Industry. The basic motto is: ***"The smaller the device, the lower the cost, the higher the performance"***. Furthermore, Gordon Moore's guiding law, stating that the number of memory bits or transistors will continue to ***double every 1.5-2years***, has provided a valuable target for the whole Semiconductor Industry.
Device scaling has been the driving force in the 80's and 90's that has propelled the semiconductor industry revenue from the 14 billion dollars level of the year 1980 to the 200 billion dollars level of the year 2000. As we enter the next decade, major limitations of the CMOS device need to be overcome. This requires the use of new materials and it also requires some fundamental changes to the basic CMOS structure. In order for the semiconductor industry to successfully undergo this massive and expensive transition, it is necessary to best utilize, in a cooperative mode, all the pre-competitive structures available anywhere in the world in the most cost effective way. As the pace of the Semiconductor Industry continues on a 2-year cycle for the introduction of new technology nodes, flawless ***execution*** is an absolute requirement.

Technology, Innovation and Manufacturing

Traditionally the semiconductor industry has introduced new technology nodes at a 3–year interval for most of its history. More specifically, DRAM products with four times (4X) the number of bits of the previous technology node have been the industry technology pace setters. The increase in the number of memory bits by 4X for every new technology node has been accomplished by the combination of three elements: ***Technology, Manufacturing*** and ***Innovation.***

Technology has contributed to the increase in the number of bits by means of scaling. All the physical parameters of a device have been reduced (scaled) in accordance to a well-defined set of equations that also determine the relation among the related electrical parameters. An area reduction of 0.5X, node to node, corresponding to a doubling (2X) in bit density, has been realized for the past 30 years.
Manufacturing has historically contributed to the increase in the number of bits by enabling progressively larger die sizes to be economically produced. Historically the die

size of DRAM has increased by 1.4X per technology node at time of introduction. Finally, ***Innovation*** (e.g., new memory cell structure, new capacitor structure, new device isolation approach, etc) has contributed to the increase in number of bits by providing the remaining 1.4X factor. In summary, the number of bits in a DRAM has increased from generation to generation due to the contribution of ***Technology, Manufacturing*** and ***Innovation*** by a factor: (2X*1.4X*1.4X)=4X.
However, **Innovation,** that drove the number of transistors per memory cell from six (6) to one and a half (1+1/2) in the 70's, has had a limited impact on DRAM memory cell size in recent years. It must be noted however, that 2 bits/cell has been accomplished by Flash memories. Furthermore, even though improvements in **Manufacturing** know-how have allowed the production of very large dice with excellent yields, placement of larger and larger dice on a wafer, does reduce the total number of available dice. This implies higher manufacturing cost per die even if a perfect wafer is produced.
Faced with the above challenges, the semiconductor industry has recently relied on **Technology** acceleration as the most effective way of continuing to increase the number of components per die in accordance with Moore's Law. In the mid-90's the pace of introduction of new technology nodes changed from the 3-year cycle to a 2-year cycle. Some companies have announced plans of even further reducing this technology introduction cycle to below 2-years. Introduction of new technology nodes on a 2-year cycle (0.5x area reduction per bit) automatically provides a doubling of components with no increase in die size. This approach has greatly benefited logic devices.

Strategy, Decision and Execution

The first thing that comes to mind when engineers think about scaling down a device is un-doubtfully how to print the features of the device by means of lithography. It is often underemphasized however that device scaling requires that all the physical and electrical parameters must be simultaneously and precisely scaled in order to harvest all the benefits of device scaling. The ability of the basic materials constituting the building blocks of the silicon gate CMOS to scale down for more than 30 years has gone beyond even the most optimistic previsions. Because of the exceptional sturdiness of the building blocks (e.g., materials) of the CMOS device and process, lithography technology has often found itself at the center of the attention as the pacesetter for the whole industry.

In the field of lithography, like in most other fields of engineering, the eternal struggle between ***evolutionary*** technology and ***disruptive*** technology has been often the single most important ***strategic*** element that conferences and symposiums have focused their attention on. While researchers intrinsically like to leapfrog to the next, more intellectually challenging technology, manufacturing engineers have always been able to push existing and well-established technologies to previously unexpected levels by means of continuous refinements and by making multiple tedious but predictable improvements. Despite all the improvements, however, eventually a ***decision*** needs to be made on the future new technology of choice since building a new infrastructure usually requires a very long time. From an overall technology perspective two examples of drastic transitions come to mind.

The ***first*** refers to the transition of the Semiconductor Industry from aluminum gate to silicon gate of the late 60's. The debate raged from about 1966 to 1972 and heated arguments on the possibility or impossibility of producing stable and reliable NMOS transistors continued throughout the industry conversion. However, once stable silicon gate NMOS transistors were finally demonstrated, the industry concentrated on execution and it grew more than 5 fold from the $2.5B level of 1972 to the $14.5B level of 1982.

The ***second*** debate raged on the transition from NMOS to CMOS. This device transition also occurred in conjunction with a set of major technology changes: From full wafer exposure tools to steppers, from wet etch to dry etch, from single metal to double metal, and so on. Once again the debate raged from approximately 1980 to 1986 but then the Semiconductor Industry concentrated on ***execution*** and it grew more than 7 fold from about the $27B level of 1986 to the $200B level by the end of the century.
It appears that the Semiconductor Industry is heading now for a ***third*** major device and technology transition in the next few years. As essentially most of the elements of this transition have been identified, it is now a question of ***execution.*** The next few years will decide whether or not the Semiconductor Industry will be successful in this transition.

Who is afraid of the "Red Brick Wall"?

The 1999 ITRS pointed out that many of the needs and requirements outline in this version of the ITRS, were turning "red" between the year 2005 and the year 2008. According to the ITRS color coding scheme, if an item is coded in red means that "Manufacturable solutions are not known". This message sent an alarm signal throughout the industry. Most of all, the viability of MOS transistors was questioned as gate oxide scaling, for instance, was reaching a fundamental limit. The main question was:" ***Why develop new complicated and expensive technologies if the transistor itself is not going to function any longer in the very near future?"***
The alarm launched by the 1999 ITRS triggered a flurry of activities throughout the Semiconductor Industry that consequently accelerated the pace at which an answer to the above question was sought and finally obtained.
The newly published 2001 ITRS shows, in fact, that many items that resided to the right of the "red brick wall" have moved to the left of it. The "wall" is not completely gone but it has become permeable.

From December 2000 to December 2001, the feasibility of constructing fully functional MOS transistors with 30nm, 20nm and 15nm gate length was reported at major conferences. Even though many aspects of the technologies necessary to make the transistor fully manufacturable still need to be refined and optimized, the results of the past year have given the Semiconductor Industry a new level of confidence in the future as the ***third*** major industry transition is approaching. The answer is: ***"Yes! Modified MOS transistors will be functional for at least two more decades".***

The role of lithography in the third transition: from strategy to execution

The lithography industry contributed to the ***first*** Semiconductor Industry transition by making full wafer imaging in a single exposure a reality. While all the process steps of the MOS process could be done then in a batch (multi-wafer) mode, imaging was intrinsically the throughput-limiting step in the whole process. Nevertheless, imaging the whole wafer in a single pass made this process cost effective.

The lithography industry subsequently mastered the technology of imaging and stepping across the wafer in a cost-effective way just in time for the ***second*** Semiconductor Industry transition. Steppers became the industry standard between 1980 and 1986. During this time imaging tools operating at 436nm wavelength became the industry workhorse. By mid-80's the first steppers imaging at 365nm became available also. The end of the 80's saw the first tools capable of imaging at 248nm wavelength delivered to several IC companies. During the 90's, the debate on the choice of the next imaging technology invigorated and yet distracted the whole industry. After the lithography innovation of the 80's, in which 3 different imaging wavelengths were demonstrated, the development activity on new imaging technologies became almost paralyzed in the 90's by the aforementioned debate and valuable ***time was forever lost***. Fortunately, the manufacturing engineers, both at the suppliers and at the IC companies, pushed the ***evolutionary*** approach beyond any expectations and ***saved*** the day for ***the whole*** Semiconductor Industry.

Finally, by the year 2000, the lithography community reached the conclusion on the sequence of wavelengths selected for future imaging technology***: 193nm, 157nm, and 13.5nm***. These wavelength transitions must occur in this decade in order to keep the whole semiconductor industry on the historical productivity pace of 25-30% cost reduction per function per year.
However, it is impossible to regain the time lost in the previous decade, a time that was not applied towards the development and implementation of these imaging technologies. As a result, unprecedented levels of coordination and efficiency are now necessary in order to ***execute*** the above sequence of conversions in imaging technology on time since there is no lack of implementations problems to be addressed and solved.
In fact, at present, imaging tools operating at 193nm wavelength still suffer from fundamental problems related for instance to the procurement of high quality CaF_2. This issue had already been identified in the mid-90's but hardly any significant action was taken at the time. Quantitative analysis of birefringence of CaF_2 was completed only last year. Design of a visible 157nm tool is still on the drawing board and industry infrastructure for 13.5nm exposure masks and tools is essentially non-existent.
There is not doubt, that in this decade the whole lithography industry must concentrate on ***execution***. Furthermore, estimate of investments required in establishing the whole infrastructure necessary for 13.5nm imaging technology is very large (~$1B). Implementation of this technology in manufacturing is not anticipated until the second

half of this decade and therefore most of the efforts on 13.5nm imaging technology has so far been carried out by consortia and cooperative organizations, as this technology is still considered as being in the pre-competitive phase. In addition, opportunities for cooperation among all of these organizations at the international level are many and are being explored. No single company or consortium can realistically allocate enough funds to successfully undergo the 3 wavelength conversions necessary for this decade. Cooperation at all levels is a must!
In the second half of this decade the Semiconductor Industry will undergo its ***third*** transition. New MOS transistor structure and a variety of new materials will be introduced. This transition, if well executed, will propel the Semiconductor Industry well though the second decade.
The whole Semiconductor Industry is counting on the lithography industry to execute and deliver according to this timetable.

Conclusions

The Semiconductor Industry has successfully undergone ***two*** major transitions, in the 70's and in the mid-80's, that have been followed by long periods of sustained growth. A ***third*** transition is approaching in the second half of this decade that promises to fuel the growth of the Semiconductor Industry well into the second decade of this century, if well executed. Many new materials and a renewed MOS structure will be necessary to revitalize the basic device capabilities. Lithography technology is a key enabler of the Semiconductor Industry. After a decade of discussions and heated debates, the lithography roadmap has been finally internationally accepted and the wavelengths of choice identified and agreed upon: ***193nm, 157nm, and 13.5nm***.
Execution is now the name if the game. As the level of investments required for the development and deployment of the overall lithography infrastructure continues to escalate with time and as execution on a tight time table is a must, it is necessary to resort to any available ***cooperation*** among consortia, supplier companies and IC companies to maintain the Semiconductor Industry on the historical ***25-30% cost reduction*** per function per year that has been, and still remains, at the ***center of its success***.